

RETURN ADDRESS STACK**ABSTRACT**

An apparatus for storing predicted return addresses of instructions being executed by a pipelined processor, the 5 apparatus includes a two part return address buffer that includes a speculative return address buffer and a committed return address buffer, both of which having multiple entries that may include predicted return addresses that have been pushed onto the return buffer.

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A B C D E F G H I J K L M N O P Q R S T U V W X Y Z